COMPOSITE DIELECTRIC LAYERS

BACKGROUND

Cross-Reference to Related Application

[0001] This application is a continuation of co-pending U.S. Patent Application No. 10/215,130, filed August 8, 2002, now Patent No. 6,674,146

Field

[0002] Integrated circuit processing and, more particularly, to the patterning of interconnections on an integrated circuit.

Background

[0003] Modern integrated circuits use conductive interconnections to connect the individual devices on a chip or to send or receive signals external to the chip. Popular types of interconnection include aluminum alloy interconnections and copper interconnections.

[0004] One process used to form interconnections, particularly copper interconnections, is a damascene process. In a damascene process, a trench is cut in a dielectric and filled with copper to form the interconnection. A via may be in the dielectric beneath the trench with a conductive material in the via to couple the interconnection to underlying integrated circuit devices or underlying interconnections. In one damascene process (a "dual damascene process"), the trench and via are each filled with copper material by, for example, a single deposition.

[0005] A photoresist is typically used over the dielectric to pattern a via or a trench or both in the dielectric for the interconnection. After patterning, the photoresist is removed. The photoresist is typically removed by an oxygen plasma (oxygen ashing). The oxygen used in the oxygen ashing can react with an underlying copper